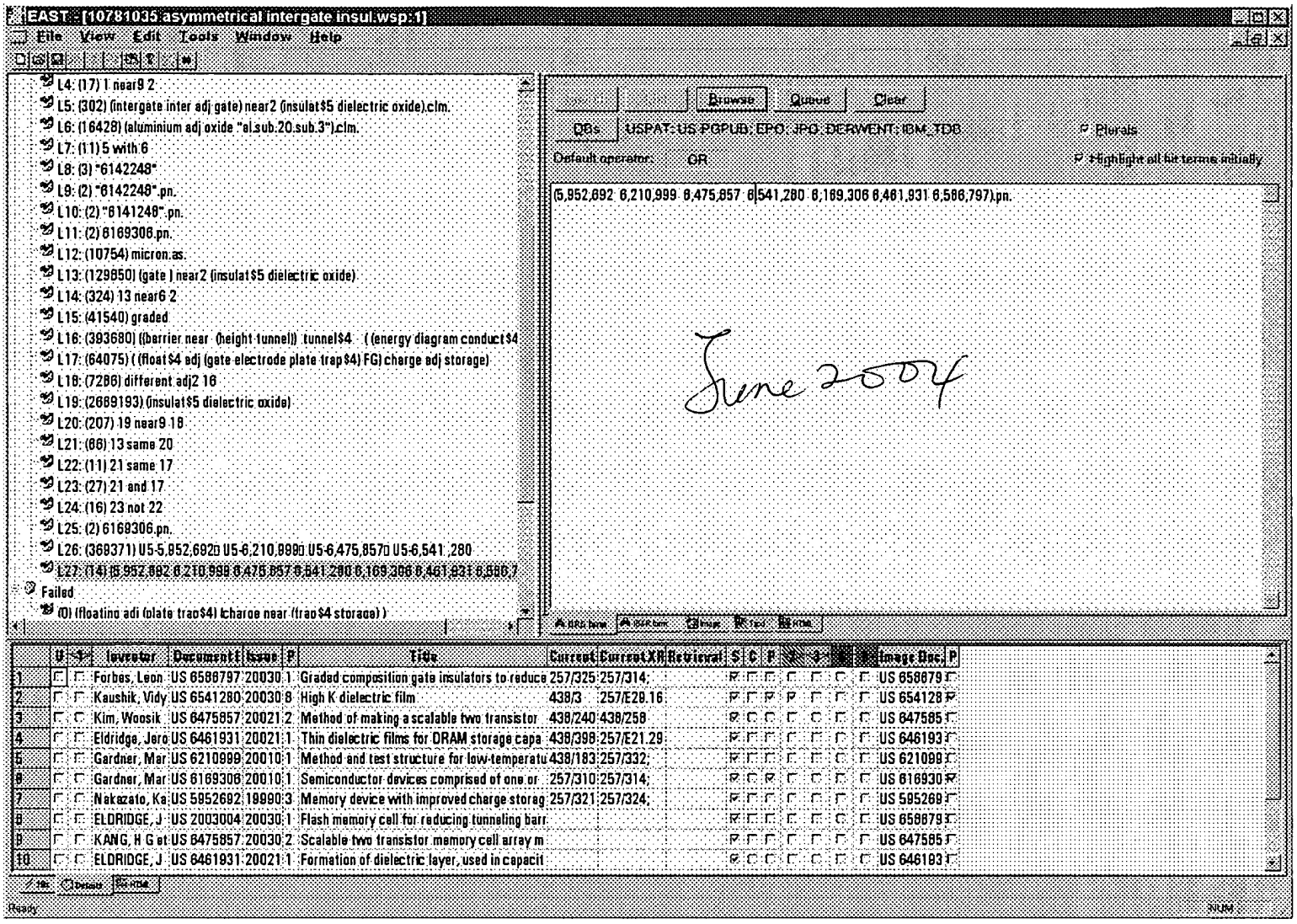
EAST: [10781035 asymmetrical intergate insul.wsp: 1]
File View Edit Tools Window Help
L4: (17) 1 near9 2
L5: (302) (intergate inter adj gate) near2 (insulat$5 dielectric oxide).clm.
L6: (16428) (aluminium adj oxide "al.sub.20.sub.3").clm.
L7: (11) 5 with 6
L8: (3) "6142248"
L9: (2) "6142248".pn.
L10: (2) "6141248".pn.
L11: (2) 6169306.pn.
L12: (10754) micron.as.
L13: (129850) (gate) near2 (insulat$5 dielectric oxide)
L14: (324) 13 near6 2
L15: (41540) graded
L16: (393680) ((barrier near (height tunnel)) tunnel$4 ((energy diagram conduct$4
L17: (64075) ((float$4 adj (gate electrode plate trap$4) FG) charge adj storage)
L18: (7286) different adj2 16
L19: (2689193) (insulat$5 dielectric oxide)
L20: (207) 19 near9 18
L21: (66) 13 same 20
L22: (11) 21 same 17
L23: (27) 21 and 17
L24: (16) 23 not 22
L25: (2) 6169306.pn.
L26: (369371) U5-5,952,692 U5-6,210,999 U5-6,475,857 U5-6,541,280
L27: (14) (5,952,692 6,210,999 6,475,857 6,541,280 6,169,306 6,461,931 6,586,7
Failed
(0) ((floating adj (plate trap$4) (charge near (trap$4 storage)))
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Plurals
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Highlight all hit terms initially
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June 2004
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1 Forbes, Leon US 6586797 20030 1 Graded composition gate insulators to reduce 257/325 257/314;
2 Kaushik, Vidy US 6541280 20030 8 High K dielectric film 438/3 257/E29.16
3 Kim, Woosik US 6475857 20021 2 Method of making a scalable two transistor 438/240 438/258
4 Eldridge, Jero US 6461931 20021 1 Thin dielectric films for DRAM storage capa 438/398 257/E21.29
5 Gardner, Mar US 6210999 20010 1 Method and test structure for low-temperatu 438/183 257/332;
6 Gardner, Mar US 6169306 20010 1 Semiconductor devices comprised of one or 257/310 257/314;
7 Nakazato, Ka US 5952692 19990 3 Memory device with improved charge storag 257/321 257/324;
8 ELDRIDGE, J US 2003004 20030 1 Flash memory cell for reducing tunneling barr
9 KANG, H G et US 6475857 20030 2 Scalable two transistor memory cell array m
10 ELDRIDGE, J US 6461931 20021 1 Formation of dielectric layer, used in capacit
US 658679
US 654128
US 647585
US 646193
US 621099
US 616930
US 595269
US 658679
US 647585
US 646193
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